Annex II

Technical Specification

- ITER_D_VH2ARW v1.0 dated 12th October 2017

for

Development of IC-Plant System Controller Prototype & Fast controller Phase 3

Development of IC-Plant System Controller Prototype Phase 3

Contract Technical Specifications

Table of Contents

1 Purpose

IC H&CD is one of Heating and Currents Drive (H&CD) systems foreseen in ITER. The IC H&CD shall provide radio-frequency (RF) heating and current drive to the ITER plasmas in the frequency range [40 MHz to 55 MHz]. A total of 20 MW of RF power in plasma is initially required from the system. The ITER IC H&CD system is composed of two antennas in port plugs, matching systems, transmission lines, RF power sources (09), HVPS (High Voltage Power Supply) (18), plant control system (IC-PSC) and test facilities (2 RF dummy loads, port plug test facilities).

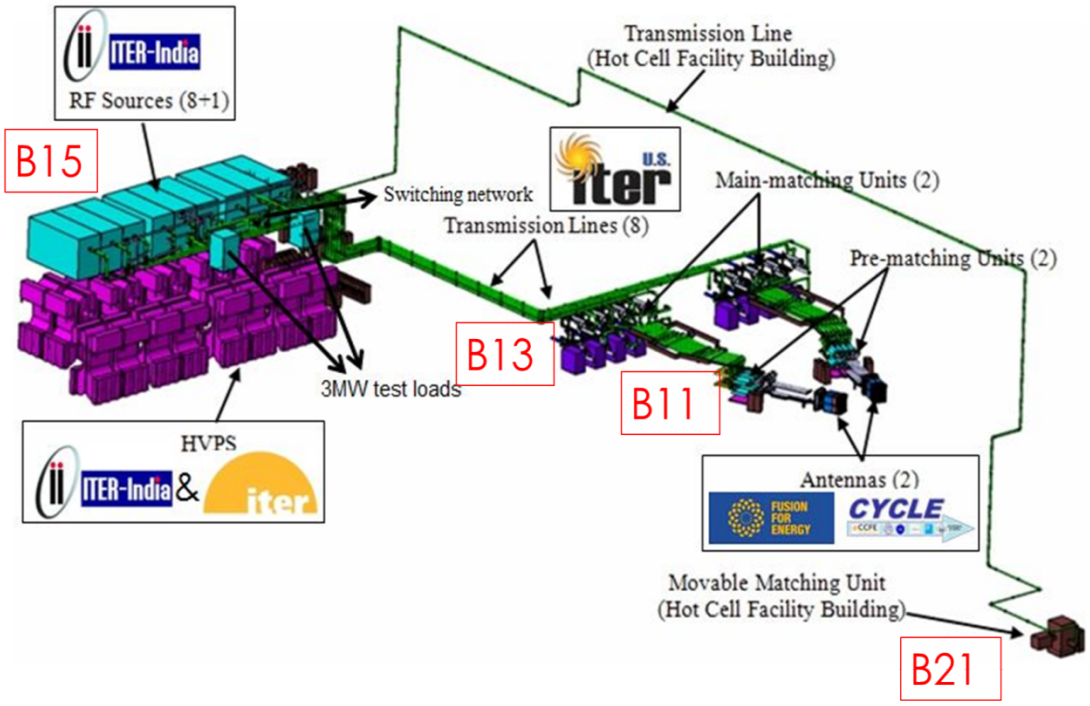


Figure 1: IC H&CD system

ICH HVPS, RF sources, TL & MS and antenna subsystems shall be procured by different procurement arrangements with different domestic agencies. HVPS, RF sources, TL & MS and antenna shall have dedicated local controllers.

IC-PSC, the Plant System Controller of IC H&CD, shall control & synchronize all local controllers.

The functional architecture scheme of the IC H&CD control system consists of this main controller (IC-PSC) controlling local/subsystem Control Units. IC-PSC provides the functional/operational interface with CODAC and the Plasma Control System, while the local Control Units controls individual subsystems (HVPSs, RF Sources, TL & MS and antenna) as illustrated in Figure 2.

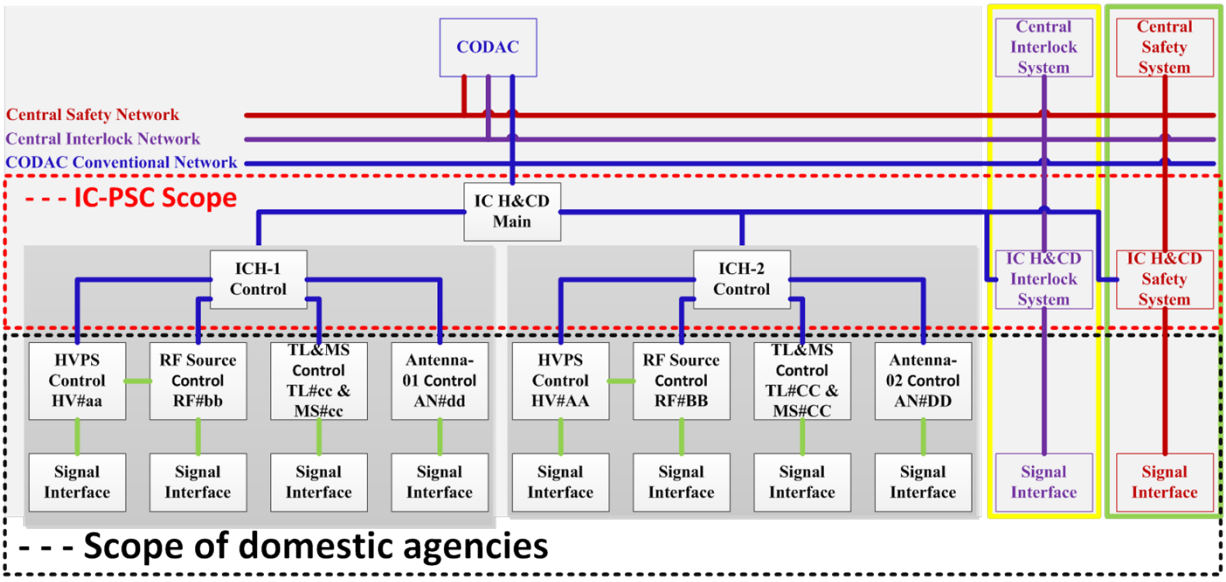


Figure 2: IC H&CD I&C Functional Architecture showing Control Hierarchy

IC-PSC, shall be procured by IO. IC-PSC has preliminary design done in January 2014, which defined functional and hardware architecture as per CODAC requirement [1]. A prototype (phase 1 and 2) was developed with CODAC in order to asses these architecture feasibility. The details of the main components of the IC-PSC prototype cubicle are given in Annex 1. The details of the work performed during the previous contract are given in Annex 2 and will be discussed during the kick off meeting. The IO TRO will guide the contractor for all that concerns the ICH system and the work done during the previous phases.

2 Scope of Work

The contract main tasks are described below. The corresponding deliverables are detailed in the chapter 6.

➔ Develop the IC PSC phase 3.

The purpose of the IC-PSC prototype located in the cubicle 20 and described in Annex 1 is to implement the functional architecture of ICH system using hardware components part of CODAC catalogue. This demonstrates that our design is compatible with CODAC core system.

On the other hand, the tools developed by CODAC team were tested and assessed. This provides essential experience of CODAC core system [1] and its subsequent evolutions.

The CODAC core system is under development process. During this phase 3 development, as for the phase 2, the contractor will have to check the updated functionalities of CODAC core system version 5.4 and if available 6.0 and propose any modifications to the existing configuration.

The work consists mainly in programming of Field-Programmable Gate Array (FPGA) card and Siemens Programmable logic controller (PLC). Core system uses EPICS as middleware for fast controller & slow controller input/output process variable access. The EPICS IOC shall be running on Red Hat Linux OS platform.

It implies as well input/ output definitions, implementation of the corresponding variables and signals in CODAC database (SDD).

Extract of the work performed during the previous phases is given in Annex 2.

➔ Define the hardware architecture of ICH PIS and PSS.

During this third phase, the contractor shall define the components that will be part of the Plant Safety System (PSS) and the Plant Interlock System (PIS). As for the conventional control components, the hardware will be chosen so that it satisfies the ICH safety and interlock function requirements. There are few functions associated to Health and Safety and interlocks in our system. They have been defined in the Hazard Identification Risk Assessment (HIRA) [2], the Interface sheet in between PBS51 and 46 and 48 [3 &4] and in some specific document that defined the SIL level of the functions [5].

The work consists in defining the hardware architecture of PIS and PSS, finding the corresponding component as per CODAC guideline and evaluating the cost of the PIS and PSS of ICH system.

➔ Implement the RF signal direct sampling process in our fast controller.

The purpose of this prototype phase 3 is to go further in the development of the RF control loop by testing the RF direct sampling method.

The progress in electronics makes possible the direct acquisition of RF measurements at the frequency of the system (35 to 65 MHz). Previously a down conversion process to lower frequency was required to allow the sampling of the signals.

CODAC provides the Linux and IO driver and application support to use direct sampling cards in the ICH System :

1. IRIO_Design_Rules_for_labVIEW_for_FPGA_QQMYTY_v1_4.pdf
2. IRIO_Library_user's_manual_RATM8Z_v1_2 .pdf
3. NI_X-Series_EPICS_Driver_User's_Guide_3P4N3R_v1_7.pdf
4. NI-RIO_EPICS_Device_Driver_User_Manual__RAJ9P8_v1_4 .pdf

This work shall be performed in close collaboration with INDA in charge of the procurement of the IC RF sources. A technical solution and the definition of which direct sampling card could be used has been proposed to INDA. We intend in IO to procure these cards and demonstrate with the corresponding implementation in our cubicle that the solution is valuable.

➔ **Prepare the installation of the cubicle in CEA to be used in the frame of the implementation of the IO test bed**

The cubicle 20 will be used in the frame of the development of the ICH test bed. For that purpose, the cubicle will have to be transferred to an external facility in CEA. The purpose of this task will be to define the component to be added to the cubicle 20 in order to be able to simulate the CODAC environment (mini CODAC) and to prepare the procedure describing the transfer process in collaboration with CODAC.

In this test bed a solid state amplifier will be installed and which will provide power up to 10 KW. With the guideline of IO TRO, the contractor will draft the control software for this component.

3 References / Terminology and Acronyms

References:

[1] **CODAC Core System Overview (34SDZ5 v5.4)**

[2] **PBS51 HIRA Final Report (Q5HT9J v1.1)**

[3] 48-51 ICD

[4] 46-51 ICD

[5] **O-003 Function specification for ICH RF leakage mitigation (R375P5 v1.1) (current)**

Definitions are given within the text.
For a complete list of ITER abbreviations see: ITER Abbreviations (ITER_D_2MU6W5).

4 Duration

The contract will have duration of 12 months

5 Responsibilities

5.1 Responsibility of ITER

ITER has the responsibility of providing detailed input data when required during the execution of the work described in Chapter 2.

Access will be granted to IDM folders to perform the tasks.

ITER shall provide offices and IT equipment at IO premises.

5.2 Responsibility of the contractor

The contractor has the responsibility of :

- regularly submitting to ITER the progress of the contract, for ITER acceptance as per chapter 7.
- implementing the IO procedures, instruction and use the corresponding templates

6 List of deliverables and due dates

The Contractor shall provide the deliverables in the form of reports. IO shall review the reports. The Contractor shall perform all the necessary modifications or iterations to the reports and submit a revised version.

Deliverables	Deliverables	Target Dates
D1	**Develop the IC PSC phase 3**: - Assess the progresses made in CODAC Core system since January 2016 (CODAC core V 5.4) - Check the relevance of the modification as regard to the IC PSC definition - Implement the functionality not already implemented in the prototype.	T0+2
D2	**ICH PIS**: - Define the functional architecture of ICH PIS - Define the hardware architecture of the ICH PIS (List of components) - Evaluate the associated cost	T0+4
D3	**ICH PSS:** - Define the functional architecture of ICH PSS - Define the hardware architecture of the ICH PSS (List of components) - Evaluate the associated cost	T0+5
D4	**IC-PSC prototype installation outside CODAC lab for ICH test bed :** Draft the software associated to the Solid State power amplifier control.	T0+7
D5	**IC-PSC prototype installation outside CODAC lab for ICH test bed :** - Establish the component required to add in the prototype in order to simulate the CODAC environment - Establish the procedure to transfer the cubicle outside	T0+8

	ITER CODAC lab.	
D6	**RF signal direct sampling:** - Assess the coding of fast controller developed in the frame of the previous contract for the RF feedback loop implementation. - Implement and program the direct sampling cards in IC-PSC prototype. The aim is to demonstrate the possibility of direct acquisition of a 65 MHz signal. The hardware required for the test will be provided by IO.	T0+10
D7	**Develop the IC PSC phase 3:** - Assess the progresses made in CODAC Core system V6.0 and implement them in the prototype software	T0+12

7 Acceptance Criteria

These criteria shall be the basis of acceptance by IO following the successful completion of the services.

These will be in the form of monthly progress reports showing the status of the deliverables detailed in Chapter 6.

Report and Document Review criteria:

Reports as deliverables shall be stored in the ITER Organization's document management system, IDM by the Contractor for acceptance.

A named ITER Organization's Contract Technical Responsible Officer is the Approver of the delivered documents.

The Approver can name one or more Reviewers(s) in the area of the report's expertise.

The Reviewer(s) can ask modifications to the report in which case the Contractor must submit a new version.

The acceptance of the document by the Approver is the acceptance criterion.

8 Specific requirements and conditions

The activities shall be driven by the IO responsible officer in the IC & LH section. The contractor's staff will work at the IO site for the duration of the contract.

- Relevant experience in technical I&C design;
- Experience in control system design, development and implementation;
- Experience in fast data acquisition and real time control
- Experience in Linux OS; C/C++, FPGA & PLC programming
- Experience in large experimental device commissioning and operation would be an advantage.
- The contractor shall have the French Electrical Authorization in order to access CODAC lab.

Up to five missions per years are planned which will be reimbursed under ITER Organization conditions.
Some work may be performed in CEA premises, in Cadarache IRFM labs, as the solid state power amplifier may be used for the ICH test bed.

9 Work Monitoring / Meeting Schedule

The work will be managed by means of Monthly Progress Meetings and/or formal exchange of documents transmitted by emails which provide detailed progress. Progress Meetings will be called by the ITER Organization, to review the progress of the work, the technical problems, the requirements, the interfaces and the planning.

The main purpose of the Progress Meetings is to allow the ITER Organization/IC&LH Section and the Contractor Technical Responsible Officer to:

a) Allow early detection and correction of issues that may cause delays;
b) Review the completed and planned activities and assess the progress made;
c) Permit fast and consensual resolution of unexpected problems;
d) Clarify doubts and prevent misinterpretations of the specifications.

In addition to the Progress Meetings, if necessary, the ITER Organization and/or the Contractor may request additional meetings to address specific issues to be resolved.

For all Progress Meetings, a document describing tasks done, results obtained, blocking points shall be written by the engineer.

All reports will be stored in the ITER IDM in order to ensure traceability of the work performed.

10 Quality Assurance (QA) requirement

The organisation conducting these activities should have an ITER approved QA Program or an ISO 9001 accredited quality system.

The general requirements are detailed in ITER Procurement Quality Requirements (ITER_D_22MFG4).

Prior to commencement of the task, a Quality Plan must be submitted for IO approval giving evidence of the above and describing the organisation for this task; the skill of workers involved in the study; any anticipated sub-contractors; and giving details of who will be the independent checker of the activities (see Procurement Requirements for Producing a Quality Plan (ITER_D_22MFMW)).
Documentation developed as the result of this task shall be retained by the performer of the task or the DA organization for a minimum of 5 years and then may be discarded at the direction of the IO. The use of computer software to perform a safety basis task activity such as analysis and/or modelling, etc. shall be reviewed and approved by the IO prior to its use, in accordance with Quality Assurance for ITER Safety Codes (ITER_D_258LKL)

11 Safety requirements

ITER is a Nuclear Facility identified in France by the number-INB-174 ("Installation Nucléaire de Base").
For Protection Important Components and in particular Safety Important Class components (SIC), the French Nuclear Regulation must be observed, in application of the Article 14 of the ITER Agreement.
In such case the Suppliers and Subcontractors must be informed that:

- The Order 7th February 2012 applies to all the components important for the protection (PIC) and the activities important for the protection (PIA).
- The compliance with the INB-order must be demonstrated in the chain of external contractors.
- In application of article II.2.5.4 of the Order 7th February 2012, contracted activities for supervision purposes are also subject to a supervision done by the Nuclear Operator.

For the Protection Important Components, structures and systems of the nuclear facility, and Protection Important Activities the contractor shall ensure that a specific management system is implemented for his own activities and for the activities done by any Supplier and Subcontractor following the requirements of the Order 7th February 2012.

Annex 1: List of components installed in the cubicle ICH 20

Fast Controller Hardware:

The following components are installed in the Cubicle-20 at CODAC Lab. These components were procured and purchased from the ICH PBS budget, hence dedicatedly belongs to the ICH section.
Fast controller component has been integrated, interfaced and tested with the CODAC tools and applications like SDD, I&C Navigator, Maven Editor, CSS etc.

Real time RF power feedback controlled algorithm written in the frame of the development of the prototype phase 1 has been tested with these fast controllers.

ICH Hardware Requirement	Number	Specification	Remarks
I&C Grade PICMG 1.3 PC 4U Computer	2	ITER specified	Integrated for ICH System
PXIe-PCIe 8371, MXI-express	2		Connection between fast controller and PXIe chassis
PXIe-1065 chassis	2	CODAC Recommendation	Integrated for ICH System
PXIe-6259 DAQ card	2	32 AI, 4 AO, 32 DIO	Integrated for ICH System
High Sampling AI PXIe-6368 Board	2	2MS/sec/Channel 16 differential AI0, 4 AO and 48 DIO.	CODAC has given temporarily for testing ICH Application.
PXI-6683(TCN Card)	2		Integrated for ICH System
SDN kit	2		Integrated for ICH System

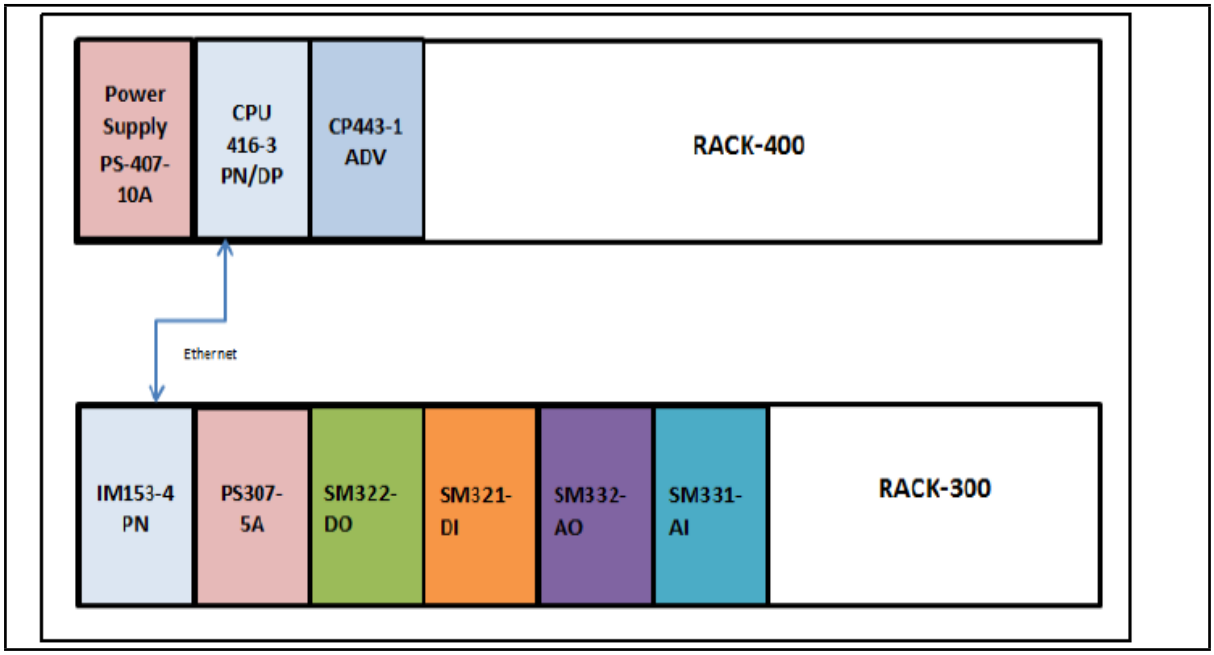
Control unit	Domain Name	Type	Comments(Configured by the CODAC for ICH-PBS51
PSH	51CICM-PSH-0002	Plant system host	51CICM-PSH-0001 as FQN
PLC	51CICM-PLC-0002	PLC host (CPU-416-3)	51CICM-PLC-CPU443-0002
PCF	51CICM-PCF-0002	PXI Fast controller	51CICM-PCF-0002

Control unit	Domain Name	Type	Comments(Configured by the CODAC for ICH-PBS51)
PSH	51CICM-PSH-0001	Plant system host	51CICM-PSH-0001 as FQN
PLC	51CICM-PLC-0001	PLC host (CPU-416-3)	51CICM-PLC-CPU443-0001
PCF	51CICM-PCF-0001	PXI Fast controller	51CICM-PCF-0002

Slow Controller hardware:

Slow controller component procured by PBS51 has been integrated, interfaced and tested with the CODAC core system tools and applications like SDD, I&C Navigator, Maven Editor, CSS etc. They are part of Cubicle-20 at CODAC Lab

All the function defined in the ICH Global Architecture document for the ICMN and ICH1 Plant control system has been implemented and tested successfully with the two set of the slow controller.



Slow Controller Network

Control unit	Domain Name	Network Address
PLC-CPU-416-3	51CICM-PLC-0001	10.201.1.124
CP-443	51CICM-PLC-CP443-0001	10.201.1.125
PLC-CPU-416-3	51CICM-PLC-0001	10.201.1.126
CP-443	51CICM-PLC-CP443-0002	10.201.1.127

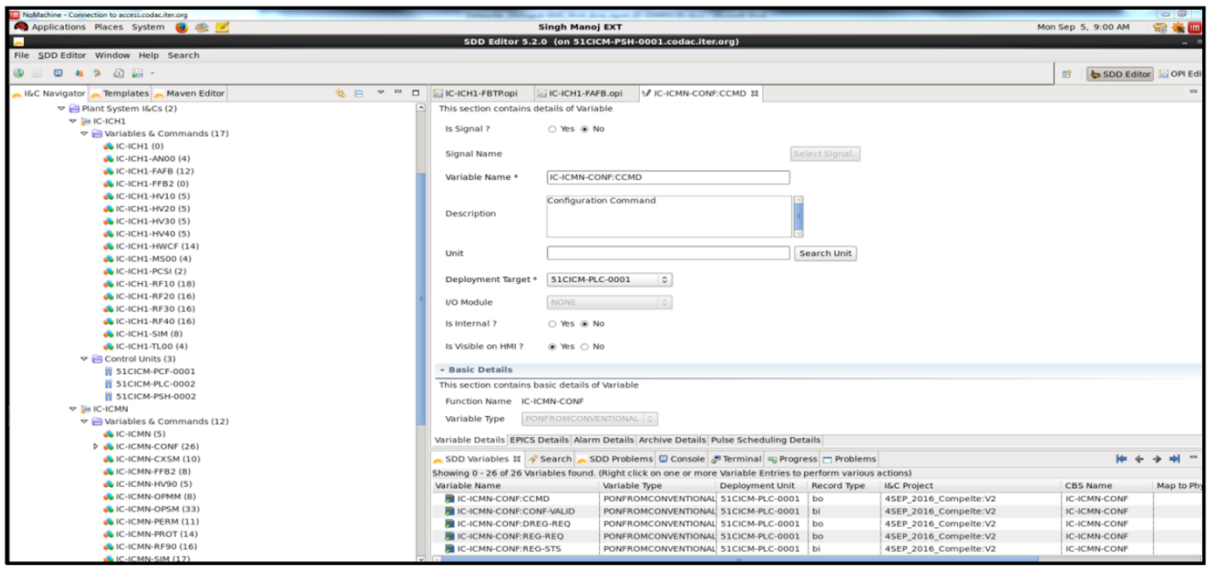
Slow Controller Hardware (2 set)

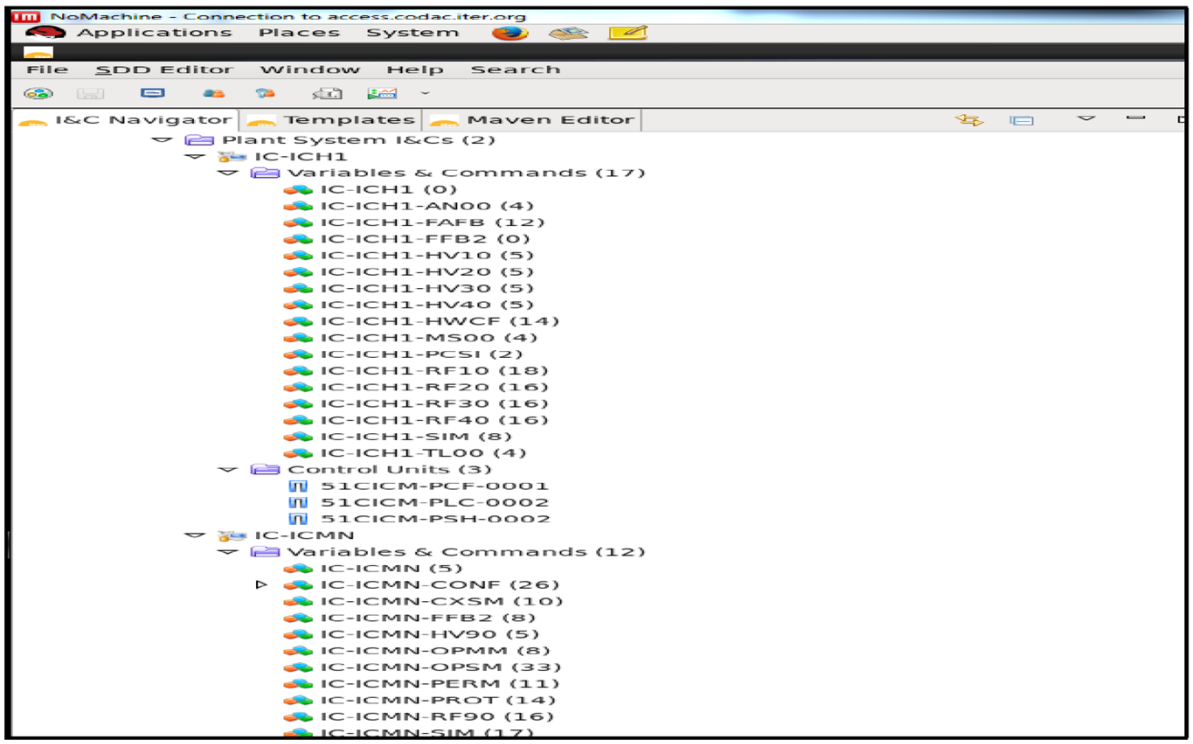
Main-Controller	**Specification**
RAIL-19IN-HS	(19inch high speed) Mounting Rail on Rack
CPU 416-3 PN/DP	(central Process unit)Main CPU
PS407-10A—supply for CPU	supply for CPU
CP443-1 ADV	Advance Ethernet Communication Processor, Ethernet board
IM Module I/O modules ET200M	
RAIL-19IN-HS	19 inch high speed. Mounting rail for IM modules
IM153-4 PN	Profinet Interface controller
PS307-5A	supply for IM
SM321- Digital Input modules	32 DI Module
SM322- Digital output modules	32 DO Module
SM331- Analog Input modules	8 AI Module
SM332- Analog Output modules	8 AO Module
SM300-AM-40P	Connector 40p for DI,DO,AO
SM300-AJ-20P	Connector 20p for AI,TC
BM-2x40	Backplane Module 2x40
Cable termination block	
Battery for S7-400	
Memory cards for s7-400	

Annex 2: Extract of the development made in the prototype PLC and fast controllers

2.5 PLC signals and variables definition in SDD-Project

In SDD-project definition two plant systems is going to be declared named as IC-ICMN and IC-ICH1 inside the I&C Navigator. Within the ICMN plant system, all the PLC function would be defined which are going to be configured, controlled and processed by the ICMN PLC. PLC programming and logic implementation has to be done from the Simatic STEP-7 programming separately. Variable declaration and compilation in SDD project would generate the Siemens PLC compatible symbol list (.SDF File) and variable list (Excel) which can be directly used in the Variable list at Siemens step-7 project file.

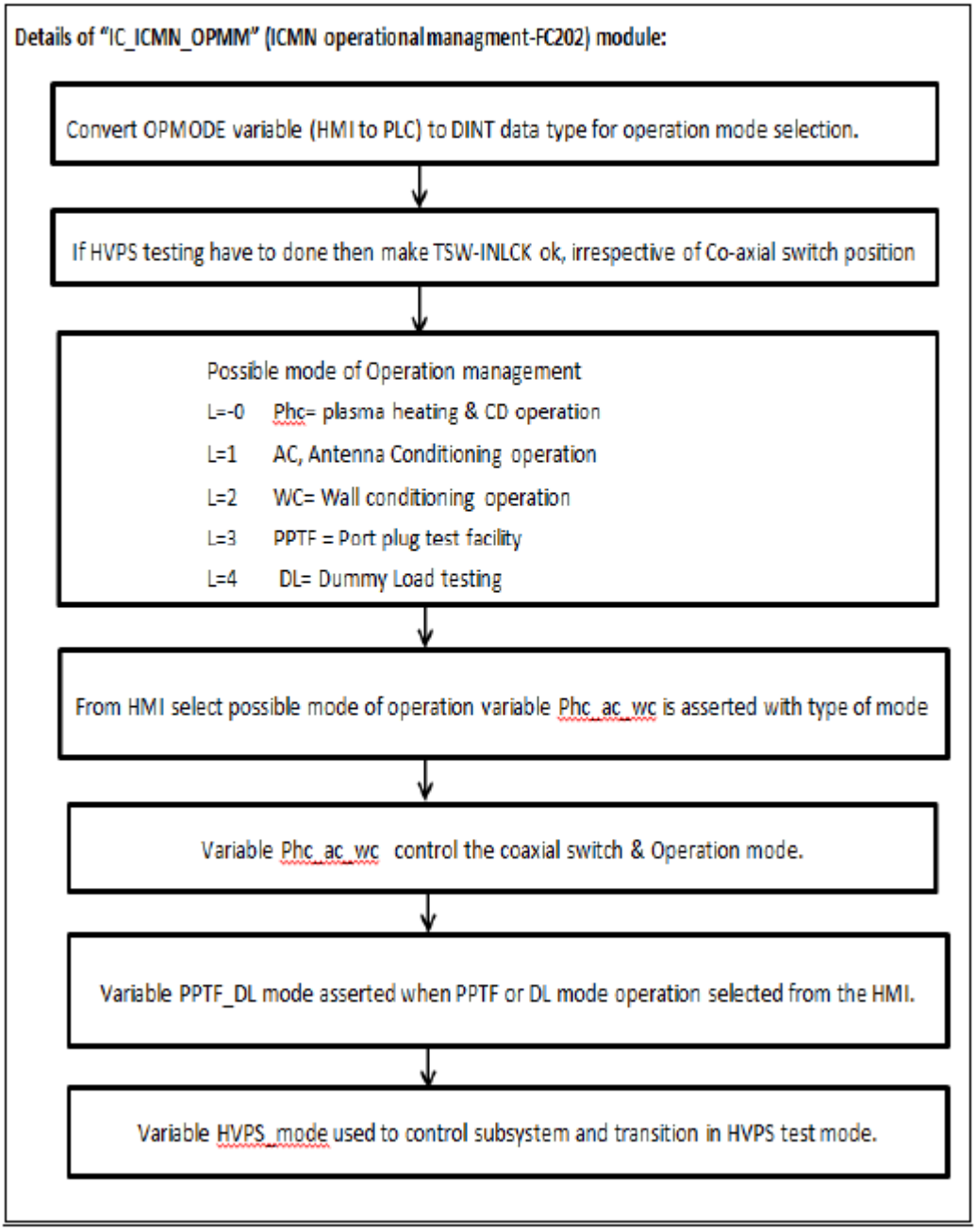




2.6 ICMN Plant Function going to implement in the PLC

2.6.1 Details of ICMN operational management module:

Flow Chart of ICMN operational management (IC_ICMN_OPMM)



Computing Code for Fast Controller

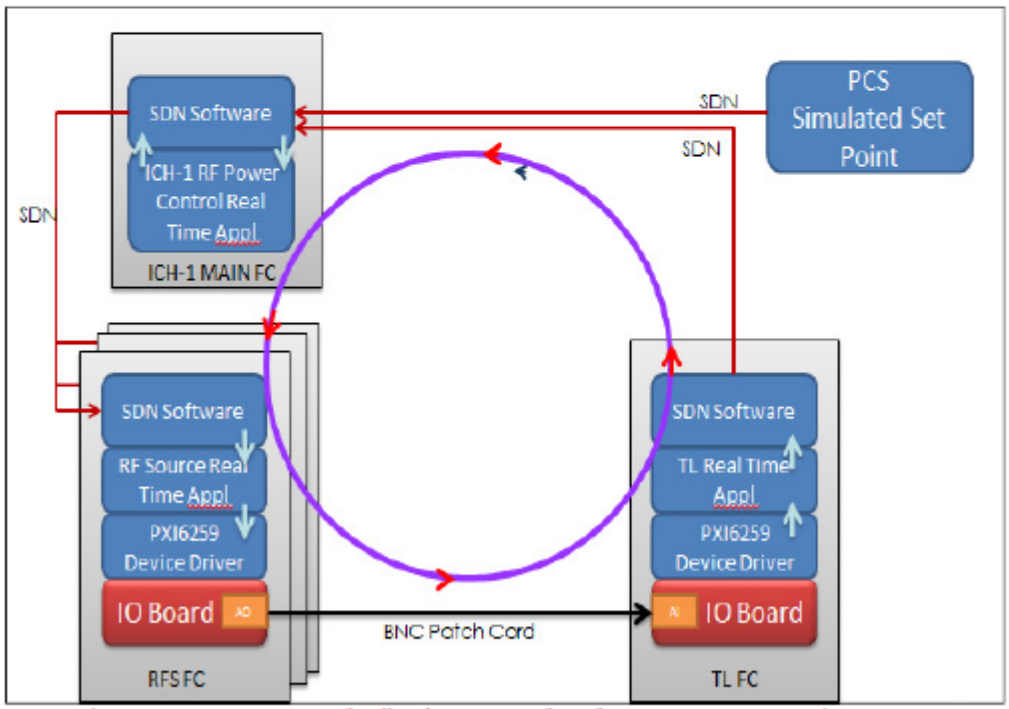
Testing Procedure of the prototype in the Fast Controller

In order to connect to the Fast Controller machines above:
1 / Open a terminal
2 / type the following command: ssh –X 51CICM-PCF-0001 / 0002
3 / 51CICM-PSH-0001
If you need to launch css, type the following command: css &.
If you need to launch sdd-editor, type the following command: sdd-editor &.
3 / To run the particular .cpp file on the fast controller following command have to enter

Fast Controller Project Name (Linux Side): 19_January

Testing of Fast Controller / PXI boards with CODAC

Example: RF Power Feedback real time loop ICH_&_CD_System_RF_Power_Feedback_Control_3G27D3_v4_1.pdf.



To test this real time RF power feedback concept, four fast controllers availability at IO required. This is not the case, so we divided full application into four different modules of C++ program. Each Program are here declared and integrated into I&C Project under the same fast controller (let it be 51CICM-PCF-0001 OR 51CICM-PCF-0002). If these application run on the same fast controller machine as per conceptually thought, then it would be run in other separate fast controller as well on SDN Network.

Application Code-1: (ICH1_PCS_SIMU.CPP): PCS-Simulation Set Point:
Application Code-2: (ICH1_TL_MSMT.CPP) Transmission line measurement:
Application Code-3 (ICH1_RF_POWER.CPP) RF Power measurement:
Application Code-4 (ICH1_PWR_CNTR.CPP): RF Power Controller:

Time Variable Power Simulation (PCS Fast Controller)

Thus maximum power demand for each pulse operation in the Tokamak machine would be set by the PCS (Plasma Control System) and communicated to ICH1 and ICH2 plant system.

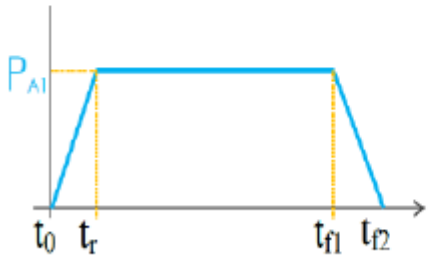
Application Code-1: ICH1_PCS_ SIMU.CPP: PCS-Simulation Set Point

In this application program, we are trying to generate and simulate the RF-power demand in real time (as would be demanded by the Plasma Control System in tokomak operation).

As shown in the Figure below, a typical time varying RF power pulse as per IDM document *[ICH & CD System RF Power Feedback Contro 3G27D3], page-8/30.*

In application program we simulated the case and Set the Power set point to demand RF Power from ICH 1/2 system (Combined RF Power from source-1 to source-4 from ICH-1 and Combined RF Power from source-5 to source-8 from ICH-2).

Table 6.2: Programmable waveforms to IC-PSC

Time variable power reference curves	IC-PSC Specifications	
	**Rise Time (t_0 - t_r) (full power)**	**200 ms**
	Flat top time (t_r - t_{f1})	3600 s (maximum)
	Fall Time (t_{f1} - t_{f2})	10 ms

To simulate the condition we had written code and generated the time varying power.

```
[ 13:24:21 ]
singhm2 @ 4501AU-SRV-0014.codac.iter.org : ~/Desktop $ ssh -X 51CICM-PCF-0001
Last login: Tue Mar 14 13:23:50 2017 from 51cicm-psh-0001.codac.iter.org
Kickstarted on 2016-11-24
CODAC Core System 5.2.0
[ 13:24:27 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~ $ cd m-27_January_2017/
[ 13:24:44 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-27_January_2017 $ ls
pom.xml  sdd.xml  src  target
[ 13:24:45 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-27_January_2017 $ cd target/bin
[ 13:24:57 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-27_January_2017/target/bin $ ls
ICH1_PCS_SIMU  ICH1_RF_POWER  ICMN_PCS_SIMU  ICMN_RF_POWER
ICH1_PWR_CNTR  ICH1_TL_MSMT   ICMN_PWR_CNTR  ICMN_TL_MSMT
[ 13:25:13 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-27_January_2017/target/bin $ ./IC
H1_PCS_SIMU
Pre-trigger time elapsing....
RF Total Power demand from PCS is = 10.000000......
RF Total Power demand from PCS is = 10.000000......
Trigger Generated....
RF Power Ramp Up in Progress........

RF Power raised in Ramp way upto 5 sample is = 2.000000......
RF Power raised in Ramp way upto 5 sample is = 4.000000......
RF Power raised in Ramp way upto 5 sample is = 6.000000......
RF Power raised in Ramp way upto 5 sample is = 8.000000......
RF Power raised in Ramp way upto 5 sample is = 10.000000......
RF Power Steady Requirements........

RF Power steady up to 5 sample is = 10.000000......
RF Power steady up to 5 sample is = 10.000000......
RF Power steady up to 5 sample is = 10.000000......
RF Power steady up to 5 sample is = 10.000000......
RF Power steady up to 5 sample is = 10.000000......


RF Power downed upto next 5 sample is = 8.000000......
RF Power downed upto next 5 sample is = 8.000000......
RF Power downed upto next 5 sample is = 8.000000......
RF Power downed upto next 5 sample is = 8.000000......
RF Power downed upto next 5 sample is = 8.000000......


RF Power Ramp Down in Progress........
RF Power is now steadied at  = 6.600000......
RF Power is now steadied at  = 5.200000......
RF Power is now steadied at  = 3.800000......
RF Power is now steadied at  = 2.400000......
RF Power is now steadied at  = 1.000000......
[ 13:25:31 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-27_January_2017/target/bin $
```

As shown in the above figure 1st five sample power is ramping from 0 to 10MW, another next 5 sample power is kept constant at 10MW, another next sample power is decreased to 8MW and kept constant at 8MW, next another 5 sample power ramping down up to 1MW. In Summary, time varying power can be simulated in the application programming.

Tx. Line Power measurement (TL-Fast Controller)
Application Code-2: (ICH1_TL_MSMT.CPP) Transmission line measurement:

This application program reads the four analog input signals form the input channels of the PXI-6259 boards. In actual system, forward and reverse power would get signals form the probe connected with the directional coupler of the transmission line.

```
[ 16:36:21 ]
singhm2 @ 4501AU-SRV-0014.codac.iter.org : ~/Desktop $ ssh -X 51CICM-PCF-0001
Last login: Wed Mar 15 16:24:17 2017 from 4501au-srv-0014.codac.iter.org
Kickstarted on 2016-11-24
CODAC Core System 5.2.0
[ 13:40:12 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~ $ cd m-6_January_2017/
[ 13:40:18 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-6_January_2017 $ cd target/bin
[ 13:40:22 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-6_January_2017/target/bin $ ./ICH1_TL_MSMT
Device opening successful

Analog Input Channel Added Successfully

Acquisition is running and pushing data over SDN Network....

********TL Measurement RT Application--New Sample taken and send to SDN*******
Received RF Power Proportional Voltage from PXI-6259 AI ch 0 is= 2.000440 V

Measured/Calculated Equivalent RF Power for TL1= 0.581162 MW

TL Power published for T10 is= 0.581162 V

Configuration Structure loaded Successfuly

Received RF Power Proportional Voltage from pxi chassis from AI ch 1 is= 4.002596 V

Measured/Calculated Equivalent RF Power for TL2= 1.186326 MW

TL Power published for T20 is= 1.186326 V

Received RF Power Proportional Voltage from pxi chassis from AI ch 2 is= 2.601021 V

Measured/Calculated Equivalent RF Power for TL3= 0.769678 MW

Pulblished RF Measurement over SDN to ICH-1 Main controller

TL Power published for T30 is= 0.769678 V

Received RF Power Proportional Voltage from pxi chassis from AI ch 3 is= 1.800998 V

Measured/Calculated Equivalent RF Power for TL4= 0.539092 MW

Pulblished RF Measurement over SDN to ICH-1 Main controller

TL Power published for T40 is= 0.539092 V

dev FD 3 has been closed

channel 3 has been closed
```

Application Code-3 (ICH1_RF_POWER.CPP) RF Power measurement:

Code-3 (ICH1_RF_POWER.CPP) RF Power measurements:

The code and logic for this application are written after getting inputs from this IDM reference- ICH_ *& CD System RF Power Feedback Contro 3G27D3-page 27/32*

9 RF power calculation example

This section describes an example of a very simple RF power calculation.

Let P_i be the RF Power output of any RF Sources where i = RF Source #1 to RF Source #9.

$$P_{RF} = P_{A1} + P_{A2}$$

P_{RF} is total IC H&CD RF power to plasma.
P_{A1} is RF power provided by ICH-1 antenna-1 at port 13.
P_{A2} is RF power provided by ICH-2 antenna-2 at port 15.

Step 1:

RF Source coefficient = depends on the RF source configuration (off line).

For example:

For ICH-1 antenna-1 at port 13:

RF Source-1, RF Source-2, RF Source-3 & RF Source-4 are configured to provide RF power.

Total power coupled to plasma by *antenna-1* be P_{A1}

For ICH-1 (antenna 1 at port cell 13) i= [1, 2, 3, 4]

Similarly for: *ICH-2 antenna-2 at port 15:*

RF Source-5, RF Source-6, RF Source-7 & RF Source-8 are configured to provide RF power.

For ICA2 (antenna 2 at port cell 15) i= [5, 6, 7, 8]

Step 2:

For ICH-1 where i= [1, 2, 3, 4]

$$P_{A1} = \sum P_i$$

Step 3: During the configuration ICH-1 sends to each RF source

$$P_i = (P_{A1} / 4)$$

Step 4: close loop feedback control can start only after $P_i > P_{min}$

Here, Pmin is minimum RF power required to start a stable feedback control

This program calculates the new set point sent to each RF source by incorporating inputs from the Transmission line, plasma control system, gain factor etc.

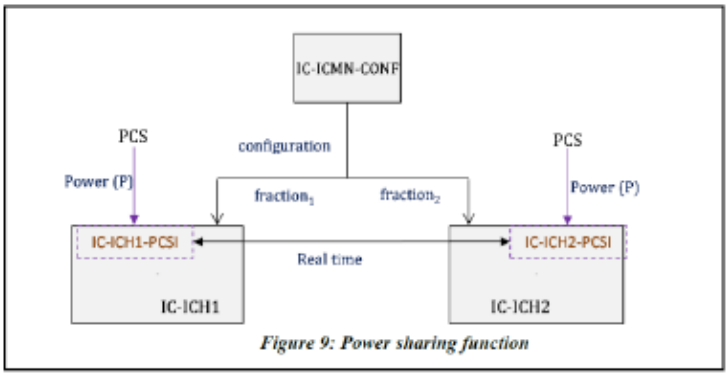


Figure 9: Power sharing function

ICH1-TL-MSMT applications reads the analog values from the PXI-6259 cards, does the necessary code process, and publish the analog values as SDN Publisher data over SDN network. This program subscribers the publish data from TL fast controller over SDN N/W and calculates the new set point as per algorithm written and sent(Publish) new set point to each RF source.

```
RF_Measurment-AI-1(TL-1 Forward power from Direction coupler)= 0.587982 MW
RF_Measurment-AI-2(TL-2 Forward power from Direction coupler)= 1.189821 MW
RF_Measurment-AI-3(TL-3 Forward power from Direction coupler)= 0.765476 MW
RF_Measurment-AI-4(TL-4 Forward power from Direction coupler)= 0.522087 MW

ICH1-TL1 Forward power from Direction coupler)= 0.000000 MW
ICH1-TL2 Forward power from Direction coupler)= 0.000000 MW
ICH1-TL3 Forward power from Direction coupler)= 0.000000 MW
ICH1-TL4 Forward power from Direction coupler)= 0.000000 MW

Received total power request from PCS(PCS-SIMulation) over SDN is= 10.000000 MW

Net ICH-1 power delivered (RFS 1 to 4) with set power ratio is= 5.000000 MW
Calculated Instantaneous RF Power Demand set point for RF10 = 1.000000 MW
Received Feedback Power from TL1 ->P1 = 0.587982 MW

Calculated Instantaneous RF Power Demand set point for RF20 = 1.400000 MW
Received Feedback Power from TL2 ->P2 = 1.189821 MW

Calculated Instantaneous RF Power Demand set point for RF30 = 1.100000 MW
Received Feedback Power from TL3(s_PW3) ->P3 = 0.765476 MW

Calculated Instantaneous RF Power Demand set point for RF40 = 1.500000 MW
Received Feedback Power from TL4(s_PW4) ->P4 = 0.522087 MW

Power Error for RF10 = -0.400000 MW
Proportional Term of PID for RF10 = -0.320000 MW
Inegration Term of PID for RF10 = -0.000320 MW
PID Output for RF10 = -0.320320 MW
```

RF Power Controller (RF Source -Fast Controller)

ICH1_PWR_Control application running on the RF source fast controller would calculate the new set point for each RF source.For calculation of new set point to Each RF Source it subscribe the SDN topic set by the ICH-1 fast controller.
Calculation is done as per written code and new set point would be sent to Power Controller unit. (Analog output signals would be available at the PXI-6259 AO terminal.

```
CODAC Core System 5.2.0
[ 16:20:41 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~ $ cd m-6_January_2017/
[ 16:20:57 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-6_January_2017 $ cd target/bin
[ 16:21:09 ]
singhm2 @ 51CICM-PCF-0001.codac.iter.org : ~/m-6_January_2017/target/bin $ ./ICH
1_PWR_CNTR
Device Successfully Opened
AO Configuration loaded Successfully for RF 1 0
AO Configuration loaded Successfully for RF 2 0
AO Configuration loaded Successfully for RF 3 0
AO Configuration loaded Successfully for RF 4 0
loop 0
channelFDs::: 13
loop 1
channelFDs::: 14
loop 2
channelFDs::: 15
loop 3
channelFDs::: 16
** New Set-point Received by RFS 10 to 40 from RF_Power_Calculation in FC****

***New Set Point Received from IC1 Main FC*****
####New RF Power Error-RF10 Sample From IC1 Main FC = 0.240000 MW ###
####New RF Power Error-RF20 Sample From IC1 Main FC = 0.360000 MW ###
####New RF Power Error-RF30 Sample From IC1 Main FC = 0.720000 MW ###
####New RF Power Error-RF40 Sample From IC1 Main FC = 0.960000 MW ###

Power set Point for RF10 from ICH-1 Main Controller = 0.330000 MW
Power set Point for RF20 from ICH-1 Main Controller = 0.660000 MW
Power set Point for RF30 from ICH-1 Main Controller = 0.550000 MW
Power set Point for RF40 from ICH-1 Main Controller = 0.990000 MW

####New RF Power Error-RF10 Sample From IC1 Main FC = 0.330404 MW ###
####New RF Power Error-RF20 Sample From IC1 Main FC = 0.097511 MW ###
####New RF Power Error-RF30 Sample From IC1 Main FC = 0.133350 MW ###
####New RF Power Error-RF40 Sample From IC1 Main FC = 0.180000 MW ###

***New Set Point Received from IC1 Main FC*****
RF Power Error for RF10 Source = 0.330404 MW
RF Power Error for RF20 Source = 0.097511 MW
RF Power Error for RF30 Source = 0.133350 MW
RF Power Error for RF40 Source = 0.180000 MW

Analog Output Voltage on PXi6259 board at channel- 1 is =  2.000000 V
Analog Output Voltage on PXi6259 board at channel- 2 is =  4.000000 V
Analog Output Voltage on PXi6259 board at channel- 3 is =  2.600000 V
Analog Output Voltage on PXi6259 board at channel- 4 is =  1.800000 V
[ 16:25:02 ]
```